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PROCESS TO FABRICATE NARROW-TRACK CPP READ HEAD

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FIELD OF THE INVENTION

The invention relates to the general field of GMR read heads with particular reference to elimination of lift-off for the critical read-width defining step.

BACKGROUND OF THE INVENTION

Conventionally, track-width and back-edge definitions of GMR heads are fabricated in two separate steps. As illustrated in FIG. 1, track width 11b is formed first through a lithographic process, followed by ion beam etching, ion beam deposition of dielectric materials, and lift-off of photo resists. Back-edge is patterned next by following the similar processes with mask 11c across the track width, as shown in FIG. 2..

FIG. 3 is a schematic representation of the area contained within circle 22, As the CPP sensor size is shrunk to below 100 nm, this conventional two-step process becomes a challenge. As noted in the area of a, b, and c in FIG. 3, such a process can produce an uneven etch-depth of dielectric materials around the sensor and cause shorting to the overlay top lead layer. One way to overcome this problem is to combine the two-step process into one by using stencil mask 41 shown in FIG. 4, which extends beyond the final

location of ABS (air bearing surface) 42. However, such modification can produce undesirable round back-edge corners 51 (as illustrated in FIG. 5). The present invention discloses an approach to resolving this problem.

In addition, conventional liftoff resist patterning procedures that employ dual- layer resists are very difficult to apply to the production of sub-100 nm resist features. The main problem lies in the very narrow process window available for undercut control. Undercut control using a thin release layer can result in liftoff difficulty. On the other hand, if the undercut is too large, it can cause collapse of the top image layer. The present invention discloses a process that eliminates the need for a liftoff mask for defining the most critical width of the structure.

A routine search of the prior art was performed with the following references of interest being found:

U.S. Patent 6,462,915 (Sasaki) discloses electroless plating of a permalloy to form the bottom pole of a CPP device.n while U.S. Patent 6,419,845 (Sasaki) shows a NiB plating layer.

SUMMARY OF THE INVENTION

It has been an object of at least one embodiment of the present invention to provide a process for manufacturing a CPP GMR read head

Another object of at least one embodiment of the present invention has been is that the GMR pillar associated with said read head measure less than about 0.1 micron on a side.

Still another object of at least one embodiment of the present invention has been that current through said read head be constrained to flow almost entirely through the layers which determine the signal strength ($\Delta R/R$) of the device.

These objects have been achieved without using a conventional liftoff process for the critical track-width defining step. Instead, the images of track width and stripe height are lithographically printed onto an intermediate layer to form a hard mask. Through this hard mask, the GMR stack can be selectively etched and then back-filled with a high-resistivity material by using newly developed electroless plating processes. Since the hard mask is insulating, the electrolessly deposited material does not form on it. The process readily adapts to a second embodiment in which current is constrained to flow through only the desired layers.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGs. 1-3 illustrate prior technology used to form a read head.

FIGs. 4-5 details some problems associated with the prior art.

FIG. 6 illustrates the first of several novel features of the present invention.

FIGs. 7-10 show how a CPP GMR pillar, measuring less than 0.1 microns on a side, can be formed according to the process of the present invention.

FIG. 9 illustrates an important feature of the present invention which is an embedding layer of high resistivity material that is electrolessly deposited.

FIGs. 12-13 show the final steps used in a first embodiment of the invention.

FIG. 14 shows the end product when using a second embodiment of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

In this invention, we disclose a method to produce a sub-100 nm CPP-structure without using the dual-layer resist lift-off process. In this method, the images of track width and stripe height are lithographically printed onto an intermediate layer to form a hard mask. Through this hard mask, the GMR stack can be selectively etched and then refilled with a high-resistivity material by using newly developed electroless plating processes.

To illustrate these ideas, we now proceed to a detailed description of the process sequence. We will use manufacture of a CPP GMR read head as a vehicle for this purpose but it will be understood that the method is more general than this and may be used whenever a feature that measures less than 0.1 microns on a side is to be carved out of a given layer.

Referring now to FIG. 6, the process of the present invention begins with the provision of bottom conductor layer 64 onto which is deposited, in succession, pinning layer 1, pinned layer 2 (a single layer of soft magnetic material or a synthetic antiferromagnetic laminate), non-magnetic spacer layer 3, and free layer 4, thereby forming GMR stack 63.

This is followed by the deposition of sputter resistant insulating layer 62 on whose

surface stripe-shaped photoresist mask 61 is formed (said stripe extending into and out of the plane of the figure and having a width between about 0.05 and 0.3 microns). Insulating layer 62 is a material such as alumina, silica, silicon nitride, or aluminum nitride and it is deposited to a thickness between about 150 and 1,000 Angstroms.

Then, as shown in FIG. 7 all of layer 62 not covered by mask 61 is removed. Then, when mask 61 is itself removed, layer 62 now becomes a hard mask of the same shape, as seen in FIG. 8. The process of etching layer 62 is now repeated with mask 61 now disposed to be orthogonal to its original orientation so that, at the conclusion of the second etching step, all that remains of hard mask 62 is the square (or rectangle if the two photoresist masks had different widths) seen in the plan view shown in FIG. 9. Also shown in FIG. 9, partly as broken lines, are the outlines of the two original photoresist masks.

Once hard mask 62 has been formed, it is now possible to use ion milling to remove as much of the unprotected portions of layer 63 as desired. In a first embodiment, ion milling is stopped once non-magnetic spacer layer 3 has been exposed, thereby forming CPP GMR pillar 63 (whose height is typically between about 200 and 500 Angstroms), as shown in FIG. 10, following which hard mask 62 is selectively removed by using EDTA (pH 9.5-10.5, 50-60 g/l at 80 °C) for alumina and aluminum nitride and RIE (CF_4, CCl_4, CHF_3, or $CHCl_3$ gas) for silica or silicon nitride.

Next, as seen in FIG. 11, embedding layer 112, of a material, whose resistivity is between about 1 and 5 milliohm cm, is selectively deposited onto the exposed surface of spacer layer 3/lower conductive layer 64 as well as on the sidewalls of CPP GMR pillar 63 to a thickness that makes its top surface coplanar with the top surface of pillar 63. Suitable materials for this purpose include, but are not limited to) NiReBP, NiReP, and NiReB. This is achieved using an electroless deposition process that will not coat insulating surfaces, following which hard mask 62 is selectively removed.

As an example, a bath having the composition listed in TABLE I could be used at a temperature between about 50 and 90 °C to deposit a material such as NiReBP, NiReP, or NiReB at a rate of about 100 to 5,000 Angstroms per minute:

Chemicals	Concentration (Moles/liter)
Nickel sulfate	0.05 to 0.2
Dimethylamine borane	0.01 to 0.05
Sodium hypophosphite	0.01 to 0.05
Sodium citrate	0.1 to 0.5
Ammonium perrhenate	0 to 0.05
Lead nitrate	0 to 10 ppm
Bath temperature	50 to 90°C
Bath pH	6 to 7

TABLE I

Once the structure of FIG. 11 has been formed, a conventional liftoff mask (not shown) is used to define areas 112a (see FIG. 12) that symmetrically extend outward from the edges of 63 for a distance large enough so that optical resolution of the liftoff mask is not a problem (typically between about 0.01 and 0.05 microns). The liftoff mask is then used for conventional subtractive etching so that all exposed portions of 112 are removed.

This is followed by the deposition of insulating layer 121 which is then lifted off, giving the structure the appearance shown in FIG. 12. Insulating layer 121 is a material such as NiReB, NiReP, or NiReBP and it is deposited to a thickness between about 200 and 500 microns. Manufacture of the read head device is then completed with the deposition of upper conductive layer 131, as shown in FIG. 13.

A second embodiment of the invention is illustrated in FIG. 14. It is similar to the just-described first embodiment except that etching of the CPP GMR layers is not terminated until pinning layer 1 has been exposed. The subtractive etching process, rather than ion milling is thus used to determine the area of layer 1, making this larger than that occupied by layers 2 and 4. This allows a larger current to pass from the lower conductive layer into the GMR stack, said larger current being then forced to flow almost entirely through layers 3 and 4 which are the ones that determine the signal strength ($\Delta R/R$) of the device.

Using known resistance values for regions 112 and 63 (in FIG. 14) the leakage (shunted) current through the embedding layer 112 is estimated to be less than 1%.

What is claimed is: